Modeling of Lead-Frame Plastic CSPs for Accurate Prediction of Their Low-Pass Filter Effects on RFICs

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Abstract **- This paper presents a direct extraction method to construct the electrical models of lead-frame plastic CSPs (Chip Scale Packages) for RFICs from the measured S parameters. To evaluate the package effects on the reciprocal passive components, the insertion loss for an on-chip 50-ohm microstrip line housed in a 32-pin BCC (Bump Chip Carrier) package was calculated based on the established package model. Excellent agreement with measurement has been found up to 15 GHz. When applied to the non-reciprocal active components, the variation of gain for an HBT (Heterojunction Bipolar Transistor) array housed in an 8-pin BCC package has been also predicted up to 22 GHz successfully. Both cases have demonstrated that the package acts as a low-pass filter to cause a sharp cut off for the RFIC components above a certain frequency.**

I. INTRODUCTION

To provide wider bandwidth in modern wireless communications, the demand for RFICs operating toward higher microwave frequencies continues growing. However, the packages are becoming a technical barrier because their parasitics are more evident to degrade RFICs as frequency increases. The conventional lead-frame plastic packages like TSSOPs and TQFPs that are currently the most often used to house RFICs have been pushed to their limits of bandwidth in many applications. Recently, lead-frame plastic CSPs such as SON (Small Outline Nonlead), QFN (Quad Flat Nonlead), LPCC (Leadless Plastic Chip Carrier) and BCC (Bump Chip Carrier) packages are gaining in popularity. These CSPs offer a smaller size than TSSOPs and TQFPs with a promising better performance at higher frequencies.

Our research was devoted to the electrical superiority of lead-frame plastic CSPs over TSSOPs and TQFPs in the applications to RFICs [1],[2]. In this paper, we have developed a complete methodology for modeling lead-frame plastic CSPs up to Ku band. The equivalent-circuit elements representing the package parasitics can be extracted from the measured S parameters directly, which has an advantage in efficiency and uniqueness over the optimization method. As an example, an electrically and thermally enhanced BCC (abbreviated to BCC^{++}) package with a pin count of 32 has been modeled. In comparison with the 32-pin TQFP, this plastic package reduces one half in the mounting footprint. From the cross-sectional sketch of the package shown in Fig. 1, the plastic package seals the semiconductor chip within the molding compound and expose the peripheral mounted pads and the center die pad on the package underside. Electrical connection between the chip and mounted pads relies on bond-wires only and such a leadless configuration can reduce the package inductance and capacitance substantially. In addition, the die pad can be soldered directly to a ground plane on the circuit board to provide excellent ground shield and thermal spread.

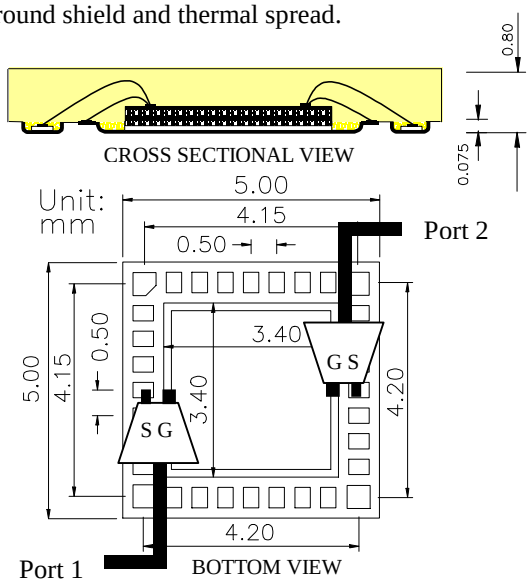

Fig. 1. Configuration of the 32-pin BCC^{++} package and illustration of its measurement with microwave probes.

II. MODELING TECHNIQUES

In the bottom view of the 32-pin BCC^{++} package as seen in Fig.1, the center die pad treated as a microwave ground is coplanar with the other peripheral mounted pads. The S parameters of an arbitrary pair of the I/O paths can be measured easily by probing the mounted pads on the bottom side of the package with a pair of fixed-pitch SG(GS)-type microwave probes connected to a vector network analyzer. Fig. 2 shows the wire-bonding configuration for the package sample with the mounted pads under test open-circuited and the corresponding equivalent model. Note that the other

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unused mounted pads are all connected to ground by down-bonding to the rim of the die pad. In the extraction, the measured S matrix $[S]^{op}$ from 1 GHz to 15 GHz is converted into the admittance matrix $[Y]^{op}$ from which the shunt and mutual capacitances C_{s1}, C_{s2}, C_m can be found as

$$[Y]^{op} = Z_0^{-1}([U]+[S]^{op})^{-1}([U]-[S]^{op}), \quad (1)$$

$$C_{s1} = median\ (\frac{\mathrm{Im}(Y_{11}^{op} + Y_{12}^{op})}{\mu}), \quad (2)$$

$$C_{s2} = median\ (\frac{\mathrm{Im}(Y_{22}^{op} + Y_{12}^{op})}{\mu}), \quad (3)$$

$$C_m = median\ (-\frac{\mathrm{Im}(Y_{12}^{op})}{\mu}), \quad (4)$$

where a median of a frequency-dependent distribution $X(f)$ is defined by a value of x such that the probability of $X(f) < x$ is less than or equal to 1/2 and the probability of $X(f) \geq x$ is also less than or equal to 1/2, for $1\mathrm{GHz} \leq f \leq 15\mathrm{GHz}$. The impedance of this measurement system, Z_0, is equal to $50\,\Omega$. Fig. 3 shows the distributions of extracted capacitance quantities corresponding to the package I/O paths (5,21). Their dependence on frequency is negligible such that only the median values have been selected for use in the model. Fig. 4 shows another package sample with the mounted pads under test wire-bonded to the die pad as well as the other unused mounted pads. In the equivalent circuit, except the same ® model of three capacitances in the front, two lossy inductances with mutual terms are included to account for the bond-wire parasitics, as also illustrated in Fig. 4. A series-parallel LR model [2] has been used to approximate the frequency-dependent losses in the range from 1 GHz to 15 GHz. In the extraction of these bond-wire parasitics, the measured S matrix $[S]^{sp}$ is first converted into the admittance matrix. After subtracting the admittance matrix $[Y]^{op}$ representing the mounted pad parasitics, we convert the admittance matrix into the impedance matrix $[Z]^{sp}$ from which the bond-wire parasitics are found as

$$[Z]^{sp} = (Z_0^{-1}([U]+[S]^{sp})^{-1}([U]-[S]^{sp}) - [Y]^{op})^{-1}, \quad (5)$$

$$L_{s1} = median\ (\frac{\mathrm{Im}(Z_{11}^{sp})}{\mu}), \quad (6)$$

$$L_{s2} = median\ (\frac{\mathrm{Im}(Z_{22}^{sp})}{\mu}), \quad (7)$$

$$L_m = median\ (\frac{\mathrm{Im}(Z_{12}^{sp})}{\mu}), \quad (8)$$

$$R_{s1} = \mathrm{Re}(Z_{11}^{sp} - Z_{12}^{sp}), \text{ at } f = 1\,\mathrm{GHz}, \quad (9)$$

$$R_{s2} = \mathrm{Re}(Z_{22}^{sp} - Z_{12}^{sp}), \text{ at } f = 1\,\mathrm{GHz}, \quad (10)$$

$$R_{p1} = (\mathrm{Re}(Z_{11}^{sp} - Z_{12}^{sp})^{-1})^{-1}, \text{ at } f = 15\,\mathrm{GHz}, \quad (11)$$

$$R_{p2} = (\mathrm{Re}(Z_{22}^{sp} - Z_{12}^{sp})^{-1})^{-1}, \text{ at } f = 15\,\mathrm{GHz}, \quad (12)$$

$$R_m = median\ (\mathrm{Re}(Z_{12}^{sp})). \quad (13)$$

The extracted and selected quantities of the equivalent circuit elements in (6)~(13) are shown in Figs. 5 and 6.

In Fig. 7 a chip with a number of bond pads on the periphery was designed to characterize chip's bond-pad parasitics. The pair of bond pads to be characterized is wire-bonded to package's mounted pads under test. The other chip's bond pads are treated as ground pads to be all connected by the U-shaped metallic patterns and then

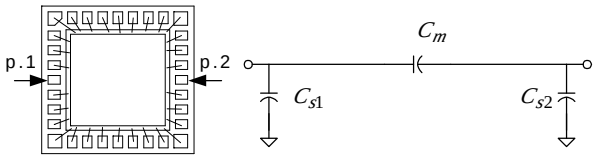

Fig. 2. Wire-bonding configuration of a test sample with single pair of I/O paths open-circuited in the package and the corresponding equivalent circuit.

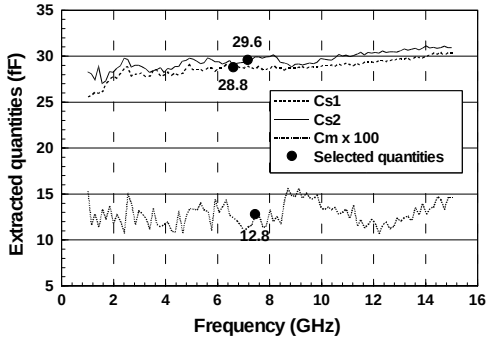

Fig. 3. Extracted and selected quantities of the mounted pad capacitances.

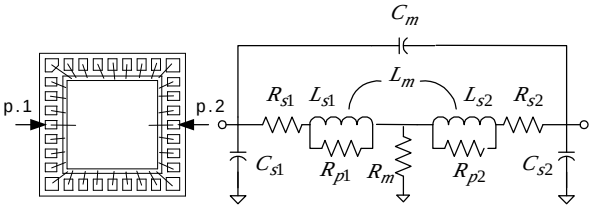

Fig. 4. Wire-bonding configuration of a test sample with all I/O paths short-circuited in the package and the corresponding equivalent circuit.

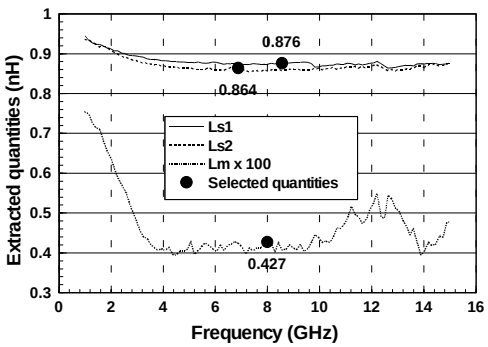

Fig. 5. Extracted and selected quantities of the bond-wire inductances.

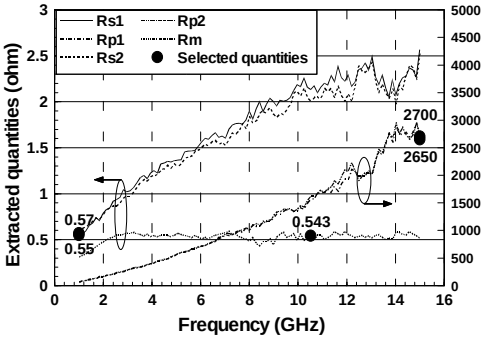

Fig. 6. Extracted and selected quantities of the bond-wire resistances.

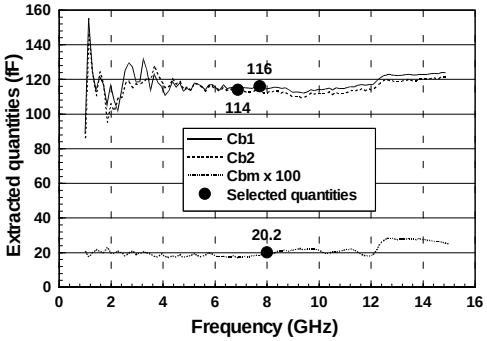

Fig. 8. Extracted and selected quantities of the bond-pad capacitances.

down-bonded to the die pad. The chip in Fig. 7 was implemented on a 10.8 mil thick GaAs substrate. Each bond pad has a dimension of 8 mil x 8 mil x 0.2 mil. The spacing between two bond pads is 2 mil. The corresponding shunt and mutual capacitances C_{b1}, C_{b2} and C_{bm} as shown in the equivalent circuit of Fig. 7 can be determined from the measured S parameters $[S]^{bp}$ using the following formulae:

$$[Y]^{ob} = ((Z_0^{-1}([U]+[S]^{bp})^{-1}([U]-[S]^{bp})-[Y]^{op})^{-1}-[Z]^{sp})^{-1}, \quad (14)$$

$$C_{b1}^{'} = \frac{\mathrm{Im}(Y_{11}^{ob}+Y_{12}^{ob})}{\mu}, \quad (15)$$

$$C_{b2}^{'} = \frac{\mathrm{Im}(Y_{22}^{ob}+Y_{12}^{ob})}{\mu}, \quad (16)$$

$$C_{b1} = median\ (\frac{L_{s1}C_{b1}^{'}C_{b1}^{''}(\mu^2-\mu_1^2)+(C_{b1}^{'}-C_{b1}^{''})}{L_{s1}(\mu^2 C_{b1}^{'}-\mu_1^2 C_{b1}^{''})}), \quad (17)$$

$$C_{b2} = median\ (\frac{L_{s2}C_{b2}^{'}C_{b2}^{''}(\mu^2-\mu_1^2)+(C_{b2}^{'}-C_{b2}^{''})}{L_{s2}(\mu^2 C_{b2}^{'}-\mu_1^2 C_{b2}^{''})}), \quad (18)$$

$$C_{bm} = median\ (-\frac{\mathrm{Im}(Y_{12}^{ob})}{\mu}), \quad (19)$$

where $C_{b1}^{''} = C_{b1}^{'}(\mu_1)$ and $C_{b1}^{''} = C_{b1}^{'}(\mu_1)$, $\mu_1 = 2\pi \times 1$ GHz. It is noted that (17) and (18) are the modified expressions of (15) and (16) respectively to exclude the influence of bond-wire's distributed capacitances in extracting bond-pad's shunt capacitances, which can yield the results with a certain degree of frequency independence, as shown in Fig. 8.

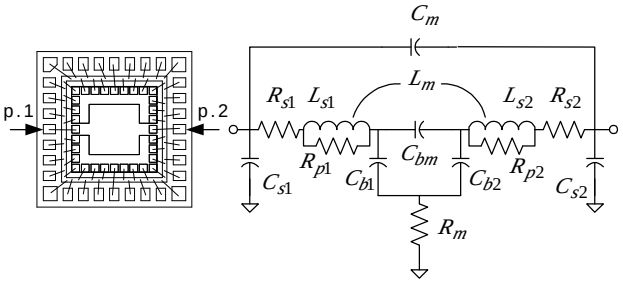

Fig. 7. Wire-bonding configuration of a test sample with a designed chip housed in the package for characterization of chip's bond pads and the corresponding equivalent circuit.

III. Evaluation of Package Effects

To evaluate the complete package effects on RFICs, one can import the S parameters for the core RFIC circuitry as a black box when cascaded with the package parasitics. For demonstration, a 50-ohm microstrip line was implemented on a 10.8 mil thick GaAs substrate and then housed in a 32-pin BCC^{++} package with a wire-bonding pattern shown in Fig. 9. This on-chip microstrip line can be regarded as embedded in two layer structure with a GaAs substrate and a molding compound superstrate. The corresponding transmission line parameters including the propagation constant γ and characteristic impedance Z_0 can be calculated using a spectral domain approach [3]. The package effects on the line are simulated based on the equivalent circuit in Fig. 9 with all element quantities selected in the above direct-extraction procedure. The calculated insertion loss has been compared to the measured results, as demonstrated in Fig. 10. Excellent agreement has been observed up to 15 GHz. One can see that the package adds a slight loss to the line below 7 GHz but causes a sharp cut off above that frequency. Such a low-pass filter effect results from the impedance mismatch due to the package parasitics. The maximum insertion loss in the passband is less than 0.5 dB. The maximum attenuation in the stopband reaches 4.2 dB at 14 GHz.

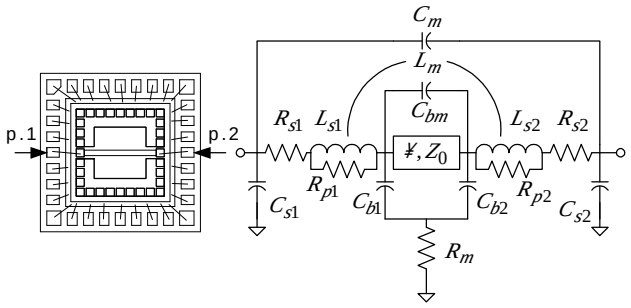

Fig. 9. Wire-bonding configuration of a test sample with an on-chip 50-ohm microstrip line housed in a 32-pin BCC^{++} package and the corresponding equivalent circuit.

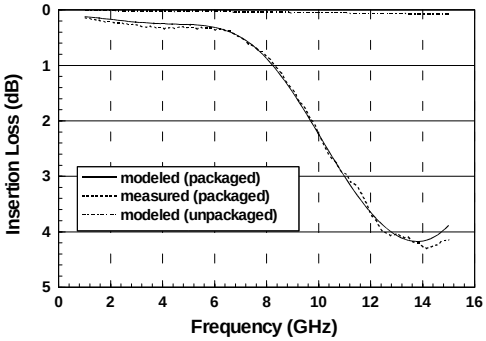

Fig. 10. Simulated and measured insertion losses for an on-chip 50 ohm microstrip line housed in a 32-pin BCC^{++} package.

In the applications to the non-reciprocal active components, we have simulated the frequency responses of GaAs HBTs housed in an 8-pin BCC^{++} package, as shown in Fig. 11. The GaAs HBTs comprise several unit cells of HBTs in an array form. Each unit cell of HBT has an emitter size of $60 \mu m^2$. The bias conditions are set at $V_{ce} = 3\text{V}$ and $J_c = 5\ \text{kA}/cm^2$. Most of the equivalent circuit elements in Fig. 11 for an 8-pin BCC^{++} package can be obtained by following the direct-extraction procedure. However, in a common emitter configuration the HBT needs to be treated as a three terminal deivce whose emitter is connected to ground pads on the chip. Down-bonding is then performed between ground pads and die pad. The associated ground-pad and bond-wire parasitics can be in general represented by a parallel $R_g L_g C_g$ resonator whose element quantities can be extracted from the S parameters measured by probing a mounted pad on the bottom side of the package that is wire-bonded to chip's ground pad. One can apply (14) to remove the influence of mounted pads and bond-wires before extraction. These ground parasitics will cause a reduction of the transistor gain, which is the so called emitter degeneration effect. Another more important factor to reduce the gain is the Miller effect due to the feedback capacitance C_{bm} whose quantity increases quite obviously after packaging. This can be explained by more coupling between the interconnections in the base and collector of the HBT array when housed in the package. The capacitance quantities C_{b1}, C_{b2}, C_{bm} can be estimated effectively from (14)-(19) with S parameters measured by probing the packaged HBT array in a reverse-biased condition. For example, Fig. 12 demonstrates the gain (S_{21}) variations from 1 GHz to 22 GHz for a $6 \times 60 um^2$ emitter-area HBT array housed in an 8-pin BCC^{++} package. One can see a low-pass filter response clearly from the curve of the packaged HBT gain normalized by the unpackaged HBT gain. In the passband, a loss close to 3 dB has been found due to a combination of Miller effect and emitter degeneration. A sharp cut off starts from 4.5 GHz. It has been inspected that the bond-wire inductances L_{s1}, L_{s2} are the dominat factors to determine the cut off frequencies. In the stopband the attenuation reaches its maximum of 12 dB at 11.6 GHz but decreases quickly above that frequency. Such a turn around in the stopband results mainly from the common-ground coupling at high frequencies. The theoretical predictions of the low-pass filter effects in Fig. 12 agree quite well with measurements.

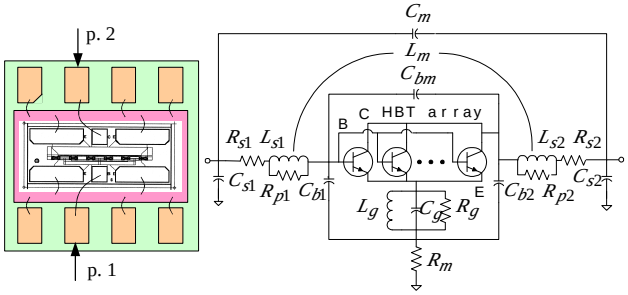

Fig. 11. Wire-bonding configuration of a test sample with an HBT array housed in an 8-pin BCC^{++} package and the corresponding equivalent circuit.

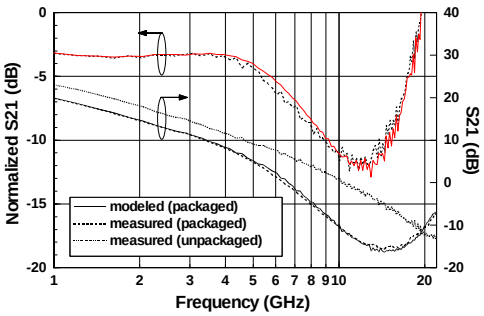

Fig. 12. Simulated and measured magnitude of S_{21} for a 6x60 um^2 HBT array housed in an 8-pin BCC^{++} package.

IV. Conclusion

A complete methodology for modeling and evaluating lead-frame plastic CSPs in housing RFICs has been presented. Two examples, an on-chip 50-ohm microstrip line and an HBT array housed in a 32-pin and 8-pin BCC^{++} package respectively, have been examined. It was concluded that the packages caused a low-pass filter effect on both components. The associated passband and stopband characteristics can be predicted precisely from the established package models.

References

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[3] O. Fordham, "Two layer microstrip transmission lines", Master's Thesis, University of California, Los Angeles, 1987.